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DC-DC Converter Dual-Bridge: A New Topology Of No Dead time DC-DC Converters*

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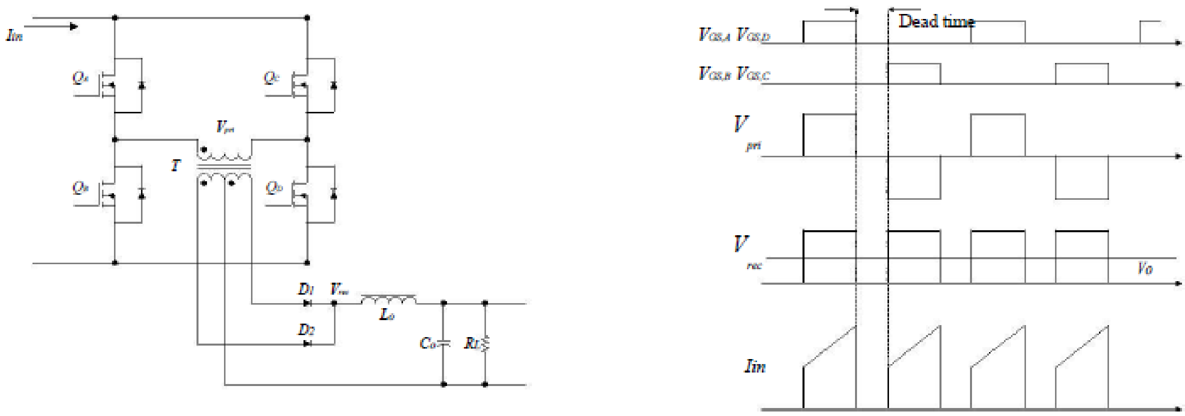
Abstract: *Two new topologies characterized by no dead time and small valued output inductor, the DC-DC converter Dual-Bridge and the Dual-Bridge converter with ZVS, are presented and analyzed. Simple self-driven synchronous rectification can be used in the new topology for high efficiency implementation. Prototype DC-DC converters have been tested for the verification of the principles. Both simulations and experiments verify the feasibility and advantages of the new topologies.*

Key Words: *dc-dc converter, Dual Bridge Converter, ZVS.*

I. INTRODUCTION

In the past decade, the performance advances of computer, telecommunication and related fields have been bringing a serious challenge to the designer of the associated power processing networks. Especially, with the widespread use of low voltage microprocessors, digital processors, as well as various low-voltage ICs, research on DC-DC converters with low voltage and high current output has become increasingly important. Rigorous requirements of fast transient response, high power density, high efficiency, high reliability and low EMI property are the targets that modern DC-DC converter design has to face.

Historically, bridge topologies are used mainly in offline converters, i.e. when twice the rectified DC would be more Than the usual switching transistors could safely tolerate. The conversion power has historically been above 500W for thefull-bridge topology. However, there is a trend to use the full bridge topology in lower conversion power ranges of 100W to 300W and lower input voltages in the tens of volts.



(a) Schematic of Power Stage of Full-Bridge Converter (b) Waveforms of Full-Bridge Converter

Fig. 1 Conventional Full-Bridge Converter

A characteristic of the conventional full -bridge converter is that it (shown in Fig. 1 are its schematic diagram and key waveforms) has a dead time during its operation. Besides preventing switches A and B (or C and D) from conducting simultaneously, this dead time is essential for conventional dual-end (half- and full-bridge, push-pull, etc.) converters to obtain a regulated output voltage when the input voltage changes. During the dead time, the input current becomes zero; this discontinuity causes a large input ripple current. Thus, large input filters must be used to satisfy the conducted EMC requirements. This dead time also needs a large output inductor to smooth the output voltage and limit the ripple current through it. The large output inductor slows the output response time.

Certain topologies have no dead time, which results in energy being continuously transmitted from the input DC source to the output load in the whole switching period. Because of the lower input ripple current in a no dead time DC-DC converter, the conducted EMI filter is relatively smaller. Lower output inductance value (this will be explained later in the paper) improves the output transient speed and reduces the output filter size, thus improving power density (power-to-volume ratio) of the DC-DC converter. Several methods, for example, magnetic transformer tapping [1] and implementation with two transformers [2][3], can bemused to realize no dead time topologies. Figure 2 shows their typical waveforms of input current *iin* and the voltage *Vp* across the primary winding of the transformer.

This research presents two topologies of no dead time DC-DC converters. They are the Dual-Bridge DC-DC converter and the Dual-Bridge converter with ZVS. The new topologies are characterized by no dead time property and have significantly reduced output filter inductors. Philips E14-3F3 cores (effective volume *Ve* = 300 mm 2) are used as the output filter inductors in the prototype DC-DC converters with 48V input and 3.3V/30A output that are built for verifying the new topologies. Comparatively, E18 size core (effective volume *Ve* = 960 mm2) must be used in the DC-DC converter built with the conventional full-bridge topology. Because no dead time is present at the secondary winding of the transformer, self-driven synchronous rectifiers can be used as output rectifiers to increase the power efficiency of the converter. This simplifies the design of rectification circuit.

Section II introduces the principle of the dual-bridge DC-DC converter. Sections III and IV present two Implementations of the new topology. The analysis and comparison of the dual -bridge converter and conventional full-bridge converter are given in Section V. Section VI gives the experimental results of the dual-bridge with ZVS and Section VII concludes the paper.

II. PRINCIPLE OF DUAL-BRIDGE DC-DC CONVERTER

The principle diagram of the proposed new topology, Dual-Bridge DC-DC converter is shown in Figure 3. The idealized illustrative waveforms of voltages and currents are listed in Figure 4.

Switches *SW1, SW2, SW3,* and *SW4* consist of a full-bridge converter. Switches *SW1, SW2* and capacitors *C1, C2* consist of a half-bridge converter. Dual-Bridge converter is the combination of the full -bridge and the half-bridge. Unlike the (interesting) circuits in [2] [3], the two bridges are connected by the fifth switch *SW5*, which eliminates the need of a second transformer required by [2] [3]. All components are assumed ideal for the convenience of description. *V1* and *V2* in Figure 3 are two 50% duty ratio complimentary control signals of switches *SW1* and *SW2* with frequency *f. V4* and *V3* are control signals of switches *SW4* and *SW3* with duty ratio
of *D* and switching frequency *f. V5* drives switch *SW5* to operate at frequency *f0 = 2f*. The switch *SW5* is turned on when both *SW3* and *SW4* are turned off.

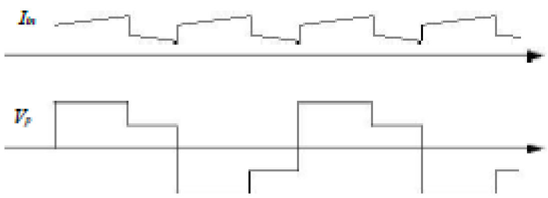


Fig. 2 Typical Waveforms of No Dead time DC-DC Converter *Iin* is input current, *Vp* is the voltage across the primary winding of the transformer

Suppose the converter works in steady state and its output inductor current is under continuous conduction mode. Referring to Fig. 4, we now describe the operation of the dual-bridge converter: For $t0 \le t \le t1$, switches *SW1* and *SW4* are turned on. The voltage *Vp* of the transformer primary winding equals the input voltage *Vi* of DC source.

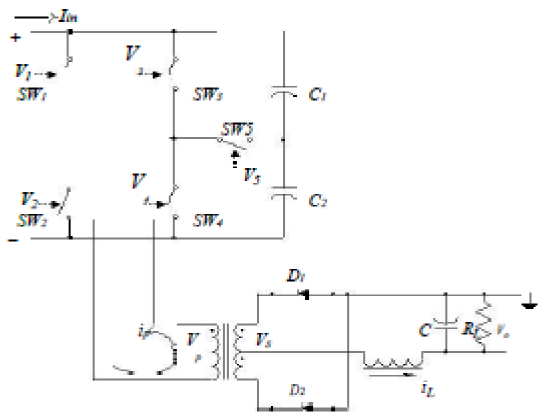


Fig. 3 Principle Illustration of Dual-Bridge Converter

During this period of time, the input current *iin* increases and equals the primary winding current *ip* and reaches to *ip,max* at time *t1*. At time *t1*, *SW4* is off and *SW5* is on. *Vp* equals *Vi /2*. From *t1* to *t2*, input current *iin* decreases from *ip,max/2*. Also, *ip*, decreasing from *ip,max*, is now supplied by *iin* and the discharging and charging currents of *C1* and *C2*. At time *t2*, *SW1* and *SW5* turn off and *SW2* and *SW3* turn on. After a very short period of
transient time, *Vp* =˜ *Vi* changes polarity, and *ip*˜ *ip,min* changes direction. Then from *t2* to *t3*, *ip* changes from ˜*ip,min* to˜ *ip,max*. At *t3*, *SW3* is off, and *SW5* turns on. Then *Vp* =˜ *Vi/2*, *iin* = *ip,max / 2*, and *ip* changes from ˜*ip,max* towards˜ *ip,min*, with *ip(t 4)* =˜ *ip,min*. From *t3* to *t4*, *ip* is supplied by i nput current *iin* and the charging and discharging currents of *C1*and *C4*. From *t4*, after a very short period of transient time, *Vp* and *ip* change polarity, and the process repeats hereafter as stated above.

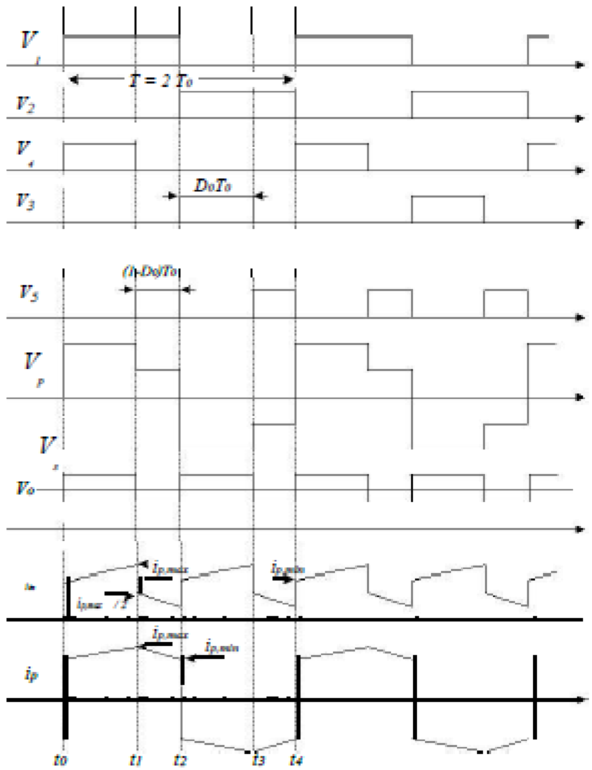
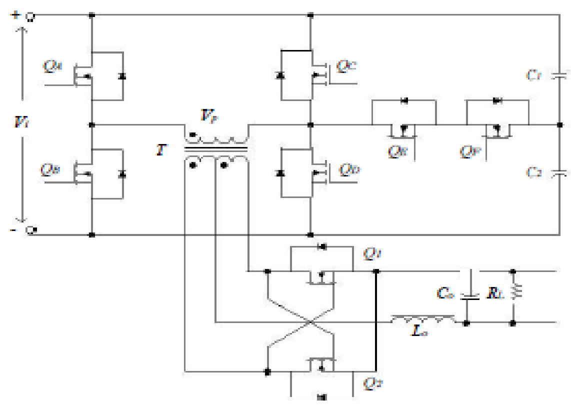
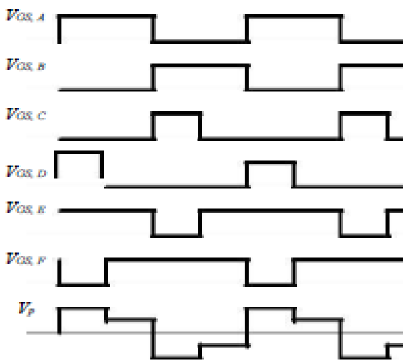


Fig. 4 Idealized Waveforms of Dual-Bridge Converter

When the dual-bridge converter operates in the abovementioned process, there is no dead time in its operation mode. That is, energy is transmitted from the input source to the output load at any given time (switch transient time is negligible compared with the operation cycle time). In this case, the range of the input voltage change *Vmax : V min* is l imited to 2:1. When the input DC voltage is *Vmin*, the duty ratio of *SW3* and *SW4* is 50%, and the duty ratio of *SW5* is 0 (SW5 is off during the whole period *T*). Then the converter operates like a full-bridge converter with 50% duty ratio. When the input DC voltage is *Vmax*, the duty ratio of *SW3* and *SW4* is 0, while the duty ratio of *SW5* is 100% (*SW5* turns on During *T*), and the converter operates like a half-bridge converter with 50% duty ratio. In these two situations, the voltage across the filter inductor *L* is zero, and the ripple current through *L* is also zero. When the input voltage Changes between *Vmin* and *Vmax*, the duty ratio of *SW3* and *SW4* change between 50% and 0, and the duty ratio of *SW5* is from 0 to 100%.

If the input voltage range is greater than 2:1, one of the schemes is, at the lower end of the input voltage range, the converter operates in full-bridge converter mode. That is, the dual-bridge converter is now a full-bridge converter consisting of switches *SW1*, *SW2*, *SW 3* and *SW4*. Switches *SW1* and *SW2* operate with less than 50% adjustable duty ratio (which is the same as the duty ratio of *SW 3* and *SW4*), while *SW5* turns off all the time. At the upper end of the input voltage range, the dual-bridge converter operates in half bridge converter mode. In this case, *SW1*, *SW2*, *C1* and *C2* consist of a half-bridge converter with *SW5* turns on, *SW 3* and *SW4* turn off all the time, while *SW1* and *SW2* operate with less than 50% adjustable duty ratio. In the middle of the input voltage range, the dual-bridge converter operates in no dead time mode as described above. For input voltage range wider than 2:1, it is possible for the dual-bridge converter to operate in no dead time mode + half-bridge mode with dead time or in full-bridge mode with dead time + no dead time mode. In this paper, the discussion to the dual-bridge converter is limited only to no dead time mode with input voltage within 2:1 range.





(a) Configuration of Dual-Bridge Converter (b) Time Sequence of Control Signals

Fig. 5 Fundamental Implementation of Dual-Bridge Converter

III. IMPLEMENTATIONS OF DUAL-BRIDGE CONVERTER

Figure 5 shows the implementation of Dual -Bridge DCDC converter. From the operation description of Dual-Bridge converter, it can be seen that *SW5* should be controlled bidirectional. To realize this, two MOSFETs *QE* and *QF* are used to function *SW5*. Switches *Q A ~ F* operate at the same frequency. *QE* is off only when *QC* is on; *QF* is off during the conduction of *QD*. The time sequences of other control signals are the same as the above-mentioned description. When the Dual-Bridge converter has a low voltage output, MOSFETs are used to form synchronous rectifiers instead of using diodes *D1* and *D2*. Because the waveform of the secondary winding of the transformer has 50% duty ratio, simple self-driven synchronous rectification method can be used in design to improve power efficiency. This significantly simplifies the design of the rectification circuit. In the case of the conventional full-bridge converter, control-driven is often used to achieve the improvement of the conversion efficiency [4].

IV. DUAL-BRIDGE DC-DC CONVERTER WITH SOFT SWITCHING PROPERTY

Although the control signals of Dual -Bridge DC-DC converter are not phase shift signals, zero voltage turn-on switching (ZVS) property can be obtained by the correct time selection of the triggering control signals of switches *QE* and *QF*, as well as the proper design of other switch control signals' time sequence. ZVS for switches *QE* and *QF* is realized independent of load condition, whereas, for other switches, it is dependent on load condition and circuit parameters (as is generally the case for ZVS realization). All capacitors in parallel with switches shown in Figure 6 are the switch output capacitance, *Coss*. Inductor *LR*, utilized as resonant inductance in transient process, may be the leakage inductance of the transformer. It may also be an external series inductance added to broaden the ZVS range.

The transfer from *QA* and *QD* on to *QA* and *QF* on (note that Q E conducts all the time in and before this interval, see Fig. 7) is treated through monitored voltage *VDS,F*. During the conduction of *QD*, *VDS,F* is positive and approximately equal to *Vin / 2*. At the end of this transfer interval, *DF*, the body diode of *QF*, conducts and *VDS,F* goes to approximately zero. Then *QF* is enabled to conduct. Though the gate control signal

of *QF* may have already arrived before *D F* conducts, it is blocked until *VDS,F* approaches zero. The transfer from *QB* and *QC* on to *Q B* and *QE* on experiences similar processes in which *QE* will not be enabled to conduct until *VDS,E* goes to approximately zero.
As stated in the implementation of the Dual-Bridge converter, this ZVS Dual-Bridge DC-DC converter can utilize the no dead time characteristic to easily accomplish self driven synchronous rectification at the output.

V. DUAL-BRIDGE CONVERTER VS. CONVENTIONAL FULL- BRIDGE CONVERTER

The reduction of magnetic component size is an effective way of improving the converter power density of a DC-DC converter. In addition, the time to respond to a change in DC load current is dependent on the size of the output inductor (a smaller value permits more rapid current changes in it) and the bandwidth of the error amplifier [5]. Usually the inductance value of the output filter is the bottleneck of increasing transient speed. Hence, how to use smaller inductance value (thus, smaller inductor size) to meet design specifications is very important to improve the performance of DC-DC converters.

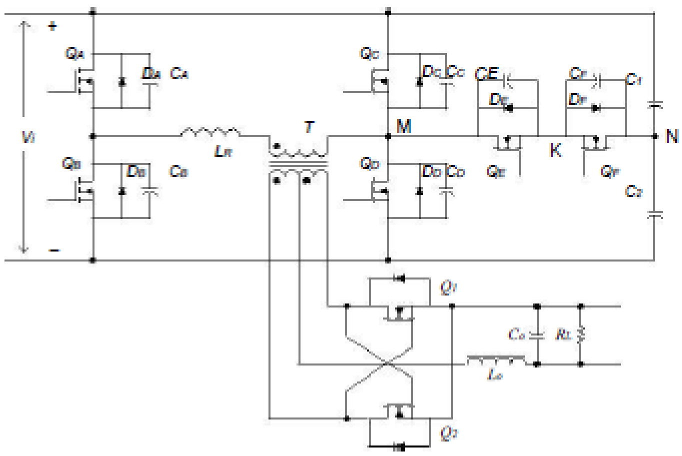


Fig. 6 Illustration of Dual-Bridge Converter ZVS Transition

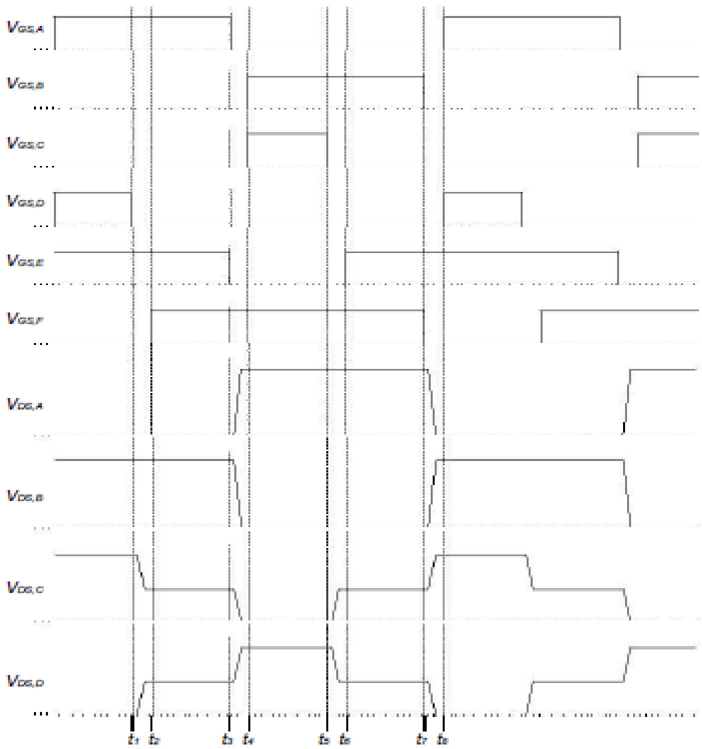


Fig. 7 Waveforms of ZVS Dual-Bridge Converter Operation

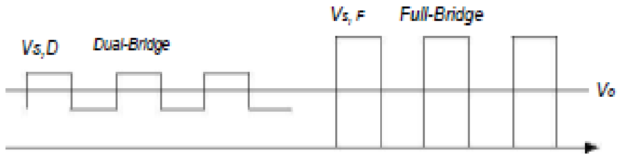


Fig 8 Voltage Waveforms of Secondary Winding Center-tapped Point of Dual- and Full-Bridge DC-DC Converters

Figure 8 shows the voltage waveforms at the secondary winding center-tapped point for both full-bridge and dual bridge converters. Obviously, with the same filter inductance value, the ripple current, which is proportional to the voltage difference Vs̃ V o, of the dual-bridge converter is much smaller than that of the full-bridge converter. The quantitative analysis is given below.
The output filter inductance value of a conventional full bridge is determined by the condition that under light load (usually, 5% ~ 10% of the full load current), the current through the inductor should keep continuous. Consider both a full-bridge converter (parameters denoted by subscripted F) and a Dual-Bridge Converter (denoted by subscripted D), with same input voltage range *Vmax*: *Vmin = 2:1*, and same output voltage *Vo*, same output current *Io*, same switching frequency *f* and period T(on output rectification waveforms *f0 = 2f*, *T0 = T/2*), duty ratio *D* (primary side of transformer), *D0 = 2D* (secondary side), turn ratio of input winding to output winding *n:1*. Comparisons of the converter characteristics, based on idealized components are made below.
<u>Full-bridge converter;</u>
At output, *V*0,*F* □*D*0,*F Vi n* , The minimum input voltage (at *D0,F = 1*) is *Vi, min = nVo* , and we have

$$n = Vi,\ min / Vo \qquad (1)$$

Peak-to-peak current on *L* for *0 < t <D0,FT0* satisfies *V sõ V* □*L*, □*ip,F*/$D_{0f,T0}$, where *Vs* is the voltage of secondary winding *Äip,F* is the peak-to peak current through the inductor.

Dmin,F = nVo / Vi max = nVo /(2 Vi, min) = 0.5., *Thus*

$$\Delta i_{p,F} = \frac{T_0 V_{i,\min}}{nL_F}\,\frac{V_i - V_{i,\min}}{V_i} \qquad (2)$$

And

$$\square I_{p,F,\max} = 0.5T_0V_0/L_F \qquad (3)$$

<u>Dual-bridge converter;</u>

$$V_o = V_s D_0 + \frac{1}{2}V_s(1 - D_0) = \frac{1}{2}(1 + D_0)V_s = \frac{V_i}{2n}(1 + D_0)\ .$$

Or $D_{0,D} = \frac{2nV_o - V_i}{V_i}$. For $D_{0,D} = 0$, we have $V_{i,\max} = 2nV_o$

For *D0,D = 1*, *Vi*,min □*nVo* and this equation is the same as ----Dual-Bridge equation (1) of full-bridge converter. Therefore, we have

$n_D = n_F = n$. Also, $V_L = V_s - V_o = L\frac{di}{dt} = L\frac{\Delta I_{p,D}}{D_{0,D}T_0}$.

Thus we have

$$\Delta i_{p,D} = \frac{D_{0,D} T_0}{nL_D}(V_i - nV_o) = \frac{V_o T_0}{L_D}\frac{(1 - D_{0,D})D_{0,D}}{1 + D_{0,D}} \qquad (4)$$

$$= \frac{T_0}{nL_D}\frac{1}{V_i}(V_{i,\max} - V_i)(V_i - V_{i,\min})$$

Let $\frac{d(\Delta i_{p,D})}{dV_i} = 0$, which is satisfied to obtain when

$$V_i\Big|_{\Delta i_{L,D,\max}} = \sqrt{V_{i,\min} V_{i,\max}} \qquad (5)$$

The peak-to-peak current through LD has maximum value, which occurs for

$$D_{0,D}\Big|_{\Delta i_{L,D,\max}} = \frac{V_{i,\max} - \sqrt{V_{i,\min}V_{i,\max}}}{\sqrt{V_{i,\min}V_{i,\max}}} = \frac{\sqrt{V_{i,\max}} - \sqrt{V_{i,\min}}}{\sqrt{V_{i,\min}}} \qquad (6)$$

And for $V_{i,man}/V_{i,\min} = 2$

$$V_i\Big|_{\Delta i_{L,D,\max}} = \sqrt{2}nV_o \qquad (7)$$

$$D_{0,D}\Big|_{\Delta i_{L,D,\max}} = \sqrt{2} - 1 \qquad (8)$$

$$\Delta i_{L,D,\max} = \left(\sqrt{2} - 1\right)^2 \frac{T_0}{L_D} V_o \qquad (9)$$

From equations (3) and (9), if the two converters have the same inductance value $LD = LF = L$, we have

$$\frac{\Delta i_{L,F,\max}}{\Delta i_{L,D,\max}} = \frac{0.5}{\left(\sqrt{2} - 1\right)^2} = 2.914 .$$

Thus, when using the same inductor as output filter, the peak-to-peak inductor current of dual-bridge converter is only approx one-third of that of conventional full-bridge converter.
If we let the two converters have the same peak-to-peak (2) current value, that is

$$\Delta i_{L,F,\max} = \Delta i_{L,D,\max} ,$$

Then LD 0.343LF . So, in this case, the inductance of the dual bridge converter is only about one-third of that of a (3) conventional full-bridge converter. Then it can be expected that the inductor current of the dual-bridge converter has slew rate approx 3 times faster than that of the full-bridge converter.

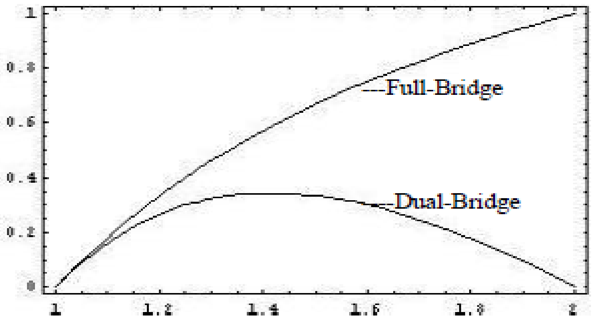


Fig. 9 Peak-to-Peak Inductor Current vs. *Vi*Where *Vi: 1~2*

Figure 9 illustrates the normalized peak -to-peak current □i p vs. input voltage Vi (1~2) for full-bridge and dual-bridge converter with the same filter inductance value. The Maximum □i p of dual-bridge is 0.343 occurs at Vi = 1.414. For full-bridge, maximum □i p = 1 at maximum input voltage Vi = 2.

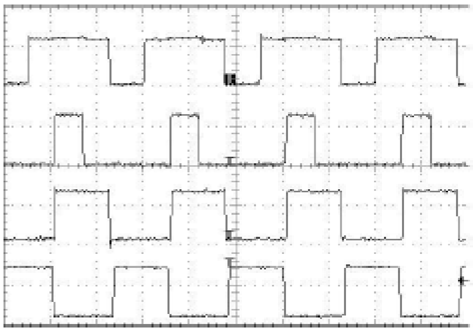


Fig. 10 Control Signals of Dual-Bridge DC-DC Converter with ZVS. From bottom trace to top trace: (10V / div) 1. VGS,A 2. VGS,B, 3. VGS,C 4. VGS, F, Time base: 2□s / div

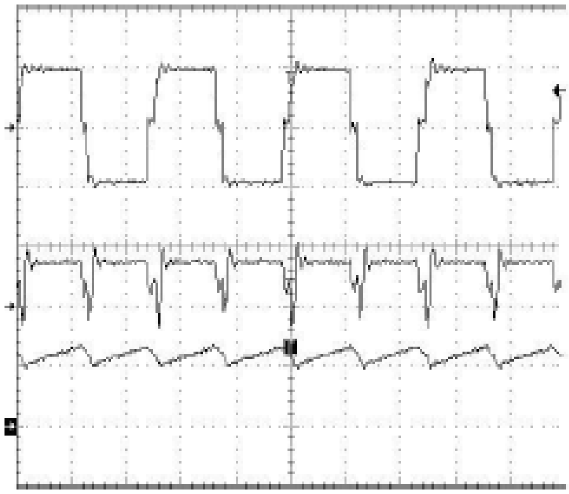


Fig. 11 Waveforms of Dual-Bridge DC-DC Converter with ZVS. Vin = 37V, Vo=3.30V, io=30A. From bottom trace to top trace: 1. iL (25A/ div) 2. Vs (5V / div) 3. VDS,D (20V / div). Time base: 2□s / div

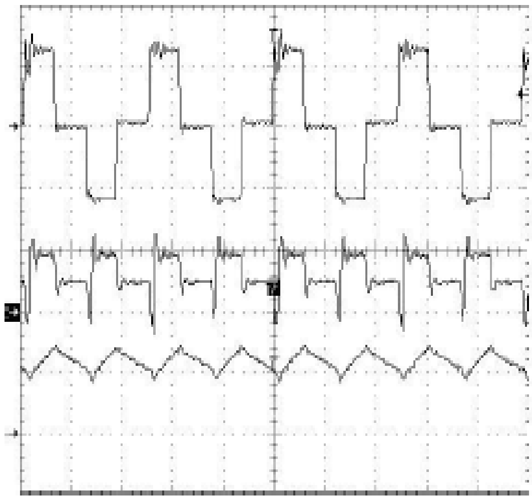


Fig. 12 Waveforms of Dual-Bridge DC-DC Converter with ZVS. Vin = 48V, Vo=3.30V, io=30A. From bottom trace to top trace: 1. iL (25A/ div) 2. Vs (5V / div) 3. VDS,D (20V / div). Time base: 2□s / div

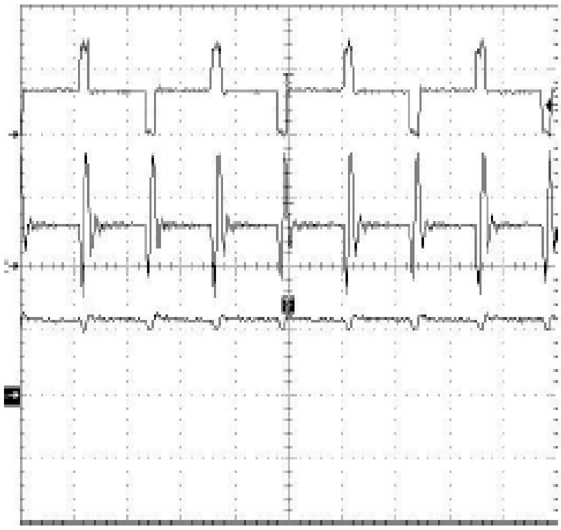


Fig. 13 Waveforms of Dual-Bridge DC-DC Converter with ZVS. *Vin* = 64*V*, *Vo*=3.30*V*, *io*=30*A*. From bottom trace to top trace: 1. *iL* (25*A*/ *div*) 2. *Vs* (5*V* / *div*) 3. *VDS,D* (50*V* / *div*). Time base: 2□*s* / *div*

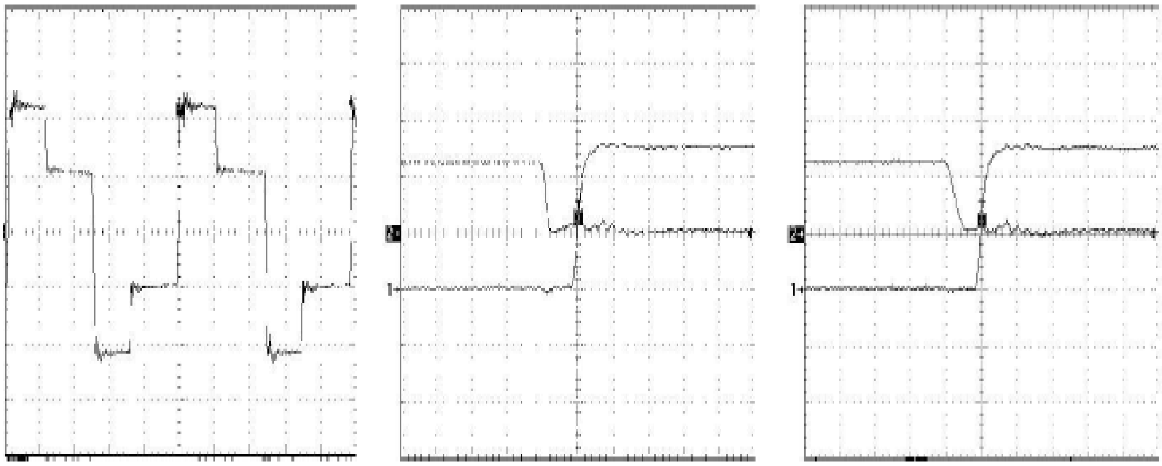


Fig. 14 Waveforms of Dual-Bridge DC-DC Converter with ZVS. *Vin* = 48*V*, *Vo*=3.30V, *io*=30*A*. Left: *Vp* (20*V* / *div*). Time Base: 1□*s* / *div* . Middle: 1. *VGS, D* (5*V* / *div*) 2. *VDS,D* (20*V* / *div*). Time Base: 100*ns* / *div* . Right: 1: *VGS,C* (5*V* / *div*) 2. *VDS,C* (20*V* / *div*). Time base: 100*ns* / *div*

VI. SIMULATION AND EXPERIMENT

Prototypes of each of the two new Dual-Bridge topologies were built with specifications: Input voltage: 48*V* (35~64*V*). Output voltage/current: 3.3*V* / 30*A*, switching frequency: 200 kHz. The magnetic core used to make transformer is Philips planar E18 –3F3 core, and the cores used for inductors are Philips planar E14 –3F3 (14x5x3.5 mm 3 , effective volume *Ve* = 300 mm 2) which is much smaller in size than E18 core (18x10x4 mm 3 , effective volume *Ve* = 960 mm 2). For a conventional full-bridge converter with the same output power, E18 size core must be used for the filter inductor. Experimental results of the ZVS dual-bridge converter are shown in Figures 10 ~ 14. The results are consistent with simulations.

Figure 10 shows the control signal waveforms. Figures 11 ~ 13 show the waveforms of (from bottom to top) the current through the output inductor, the secondary winding voltage after rectification and *VDS,D*, with 3.3*V* 30*A* output under 37*V*, 48*V* and 64*V* input voltages, respectively. Fig. 14 illustrates the ZVS operation, in which the drain-source voltage falls to zero before the rising edge of the gate-source voltage of the corresponding switch arrives. Efficiencies under different load current (20 *A* and 30*A*) are given in Fig. 15. Theefficiency curves are for a prototype only, and the design is not yet optimized for power efficiency.

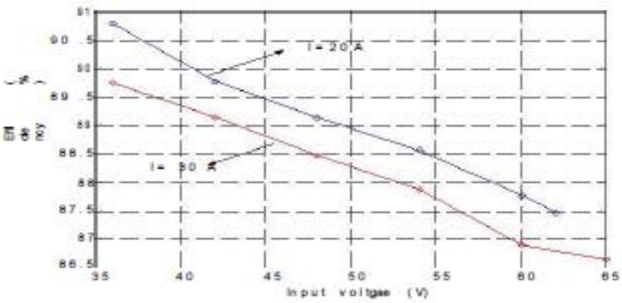


Fig. 15 Efficiency of Dual-Bridge Converter at *io* = 20A and *io* = 30A

VII. CONCLUSION

Two new topologies of no dead time DC-DC converters are presented and analyzed. The new topologies have been verified by both simulation and experiments (although experimental results are only presented for the dual –bridge with ZVS in this paper, due to lack of space) . The output filter inductors were built with planar E14-3F3 core for 100 *Watts* output power and are significantly reduced in both size and inductance value, compared with the inductor of full bridge DC-DC converter. For the latter, usually an E18 size core has to be used for the same output power.

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